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APPLICATION NO.	FILING DATE	FIRST NAMED INVENTOR	ATTORNEY DOCKET NO.	CONFIRMATION NO.
10/759,330	01/15/2004	Elias Gedamu	200209681-1	7714

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EXAMINER	
CONTINO, PAUL F	

ART UNIT	PAPER NUMBER
2114	

DATE MAILED: 08/03/2006

Please find below and/or attached an Office communication concerning this application or proceeding.

Office Action Summary	Application No.	Applicant(s)	
	10/759,330	GEDAMU, ELIAS	
	Examiner	Art Unit	
	Paul Contino	2114	

-- The MAILING DATE of this communication appears on the cover sheet with the correspondence address --

Period for Reply

A SHORTENED STATUTORY PERIOD FOR REPLY IS SET TO EXPIRE 3 MONTH(S) OR THIRTY (30) DAYS, WHICHEVER IS LONGER, FROM THE MAILING DATE OF THIS COMMUNICATION.

- Extensions of time may be available under the provisions of 37 CFR 1.136(a). In no event, however, may a reply be timely filed after SIX (6) MONTHS from the mailing date of this communication.
- If NO period for reply is specified above, the maximum statutory period will apply and will expire SIX (6) MONTHS from the mailing date of this communication.
- Failure to reply within the set or extended period for reply will, by statute, cause the application to become ABANDONED (35 U.S.C. § 133). Any reply received by the Office later than three months after the mailing date of this communication, even if timely filed, may reduce any earned patent term adjustment. See 37 CFR 1.704(b).

Status

1)☒ Responsive to communication(s) filed on *15 January 2004*.

2a)☐ This action is **FINAL**. 2b)☒ This action is non-final.

3)☐ Since this application is in condition for allowance except for formal matters, prosecution as to the merits is closed in accordance with the practice under *Ex parte Quayle*, 1935 C.D. 11, 453 O.G. 213.

Disposition of Claims

4)☒ Claim(s) *1-13* is/are pending in the application.

4a) Of the above claim(s) _____ is/are withdrawn from consideration.

5)☐ Claim(s) _____ is/are allowed.

6)☒ Claim(s) *1-13* is/are rejected.

7)☐ Claim(s) _____ is/are objected to.

8)☐ Claim(s) _____ are subject to restriction and/or election requirement.

Application Papers

9)☐ The specification is objected to by the Examiner.

10)☒ The drawing(s) filed on *15 January 2004* is/are: a)☒ accepted or b)☐ objected to by the Examiner.

Applicant may not request that any objection to the drawing(s) be held in abeyance. See 37 CFR 1.85(a).

Replacement drawing sheet(s) including the correction is required if the drawing(s) is objected to. See 37 CFR 1.121(d).

11)☐ The oath or declaration is objected to by the Examiner. Note the attached Office Action or form PTO-152.

Priority under 35 U.S.C. § 119

12)☐ Acknowledgment is made of a claim for foreign priority under 35 U.S.C. § 119(a)-(d) or (f).

a)☐ All b)☐ Some * c)☐ None of:

1.☐ Certified copies of the priority documents have been received.

2.☐ Certified copies of the priority documents have been received in Application No. _____.

3.☐ Copies of the certified copies of the priority documents have been received in this National Stage application from the International Bureau (PCT Rule 17.2(a)).

* See the attached detailed Office action for a list of the certified copies not received.

Attachment(s)

1) ☒ Notice of References Cited (PTO-892)
2) ☐ Notice of Draftsperson's Patent Drawing Review (PTO-948)
3) ☒ Information Disclosure Statement(s) (PTO-1449 or PTO/SB/08) Paper No(s)/Mail Date _____.
4) ☐ Interview Summary (PTO-413) Paper No(s)/Mail Date. _____ .
5) ☐ Notice of Informal Patent Application (PTO-152)
6) ☐ Other: _____.

DETAILED ACTION: Non-Final Rejection

Double Patenting

1. The nonstatutory double patenting rejection is based on a judicially created doctrine grounded in public policy (a policy reflected in the statute) so as to prevent the unjustified or improper timewise extension of the "right to exclude" granted by a patent and to prevent possible harassment by multiple assignees. A nonstatutory obviousness-type double patenting rejection is appropriate where the conflicting claims are not identical, but at least one examined application claim is not patentably distinct from the reference claim(s) because the examined application claim is either anticipated by, or would have been obvious over, the reference claim(s). See, e.g., *In re Berg*, 140 F.3d 1428, 46 USPQ2d 1226 (Fed. Cir. 1998); *In re Goodman*, 11 F.3d 1046, 29 USPQ2d 2010 (Fed. Cir. 1993); *In re Longi*, 759 F.2d 887, 225 USPQ 645 (Fed. Cir. 1985); *In re Van Ornum*, 686 F.2d 937, 214 USPQ 761 (CCPA 1982); *In re Vogel*, 422 F.2d 438, 164 USPQ 619 (CCPA 1970); and *In re Thorington*, 418 F.2d 528, 163 USPQ 644 (CCPA 1969).

A timely filed terminal disclaimer in compliance with 37 CFR 1.321(c) or 1.321(d) may be used to overcome an actual or provisional rejection based on a nonstatutory double patenting ground provided the conflicting application or patent either is shown to be commonly owned with this application, or claims an invention made as a result of activities undertaken within the scope of a joint research agreement.

Effective January 1, 1994, a registered attorney or agent of record may sign a terminal disclaimer. A terminal disclaimer signed by the assignee must fully comply with 37 CFR 3.73(b).

2. Claims 1, 2, 3, 7, 8, 9, and 11 are provisionally rejected on the ground of nonstatutory obviousness-type double patenting as being unpatentable over claims [1,13,17], [5,15], 6, [8,13,15], 9, 10, and 13, respectively, of copending Application No. 10/759,373. Although the conflicting claims are not identical, they are not patentably distinct from each other because the determination that a cache within a processor has failed implies that the processor itself has failed.

This is a provisional obviousness-type double patenting rejection because the conflicting claims have not in fact been patented.

Claim Rejections - 35 USC § 101

35 U.S.C. 101 reads as follows:

> Whoever invents or discovers any new and useful process, machine, manufacture, or composition of matter, or any new and useful improvement thereof, may obtain a patent therefor, subject to the conditions and requirements of this title.

3. Claims 7-13 are rejected under 35 U.S.C. 101 because the claimed invention is directed to non-statutory subject matter.

Claim 7 discloses a "system" and "modules" for carrying out the Applicant's invention. The terms "system" and "modules" as defined in the Applicant's Specification (paragraph [0024]) may be interpreted as being embodied as software and a computer language. Software and computer languages in and of themselves are not interpreted as statutory and therefor may not be patented. Claims 8-10 are rejected based upon their dependence to claim 7.

Claim 11 discloses a "computer-readable medium" where the Applicant's Specification discloses that such a medium may comprise means to "transport, propagate, or transport" a program, may be an "optical, electromagnetic," or "infrared" medium, "an electrical connection having one or more wires," "an optical fiber," and could even be "paper" or another medium in which a "program is printed". Such "computer-readable media" as claimed in light of the Applicant's Specification is interpreted as non-statutory and therefor may not be patented. Claim 12 is rejected based upon its dependency to claim 11. In order to overcome the rejection, the Examiner recommends the Applicant amend the language "computer-readable medium" to read

"computer-readable memory" – the term "memory" as disclosed throughout the Applicant's Specification is interpreted as statutory.

Claim 13 discloses a "system" and "means" for carrying out the Applicant's invention. The terms "system" and "means" as defined in the Applicant's Specification (paragraph [0024]) may be interpreted as being embodied as software and a computer language. Software and computer languages in and of themselves are not interpreted as statutory and therefor may not be patented.

Claim Objections

4. Claim 1 is objected to because of the following informalities: line 5 is more appropriate with the word "of" preceding "wafers". Appropriate correction is required.

Claim Rejections - 35 USC § 102

The following is a quotation of the appropriate paragraphs of 35 U.S.C. 102 that form the basis for the rejections under this section made in this Office action:

> A person shall be entitled to a patent unless –
>
> (e) the invention was described in (1) an application for patent, published under section 122(b), by another filed in the United States before the invention by the applicant for patent or (2) a patent granted on an application for patent by another filed in the United States before the invention by the applicant for patent, except that an international application filed under the treaty defined in section 351(a) shall have the effects for purposes of this subsection of an application filed in the United States only if the international application designated the United States and was published under Article 21(2) of such treaty in the English language.

5. Claims 1-3, 5-9, 11, and 13 are rejected under 35 U.S.C. 102(e) as being unpatentable over Song et al. (U.S. Patent No. 6,842,866).

As in claim 1, Song et al. discloses a method for testing cache performance of a processor design, the method comprising:

searching a file that contains cache test results for a lot of wafers *(column 5 lines 2-16 and 31-39, where stated the "lot of wafers" is interpreted as "a 'lot of wafers'", and not "'a lot' of wafers")*; and

determining at least one cache array location in at least one processor in the lot [of] wafers processor for which a cache test has failed *(column 5 lines 3-6 and 17-55)*.

As in claim 2, Song et al. discloses searching the file comprises parsing the file *(column 5 lines 18-55, where the analysis of the defect file and specification of particular wafers/devices to layout is interpreted as parsing)*.

As in claim 3, Song et al. discloses searching the file comprises opening the file and parsing the file *(column 5 lines 18-55, where it is necessary to open the defect file in order to process the stored data)*.

As in claim 5, Song et al. discloses developing a cache array repair signature based on the at least one cache array location for which a cache test has failed *(column 6 lines 18-17, where a black box is interpreted as a signature identifying the location to be repaired)*.

As in claim 6, Song et al. discloses the cache array repair signature defines a cache array location associated with the processor design which has failed the cache test in a statistically relevant percentage of the processors in the lot *(column 6 lines 33-61)*.

As in claim 7, Song et al. discloses a system for testing cache performance of a processor design, the system comprising:

a parser module for searching a file that contains cache test results for a lot of wafers *(column 5 lines 18-55, where the analysis of the defect file and specification of particular wafers/devices to layout is interpreted as parsing)*;

a composite repair failure identification module for determining cache array locations for which a cache test has failed *(column 6 lines 18-17, where a black box is interpreted as a signature identifying the location to be repaired)*; and

a cache array repair signature module for determining at least one cache array location associated with the processor design which has failed the cache test in a statistically relevant percentage of the integrated circuits in the lot *(column 5 lines 3-6 and column 6 lines 18-61)*.

As in claim 8, Song et al. discloses the parser module is configured to open the file that contains the cache test results *(column 5 lines 18-55, where it is necessary to open the defect file in order to process the stored data)*.

As in claim 9, Song et al. discloses the composite repair failure identification module, and the cache array repair signature module comprise software that is executed by a processor *(column 4 line 66 through column 5 line 9 and column 5 lines 17-20 and 30-39)*.

As in claim 11, Song et al. discloses a cache yield analysis program embodied in a computer-readable medium, the program comprising:

logic configured to search a file that contains test results for a lot of wafers and determine cache array locations for processors in the lot for which a cache test has failed *(column 5 lines 18-55)*; and

logic configured to determine a cache array repair signature that defines at least one cache array location associated with the processor design which has failed the cache test in a statistically relevant percentage of the processors in the lot *(column 5 lines 3-6 and column 6 lines 18-61)*.

As in claim 13, Song et al. discloses a system for testing cache performance of a processor design, the system comprising:

means for searching a file that contains test results for a lot of wafers *(column 5 lines 18-55)*;

means for determining cache array locations for processors in the lot for which a cache test has failed *(column 6 lines 18-17, where a black box is interpreted as a signature identifying the location to be repaired)*; and

means for generating a cache array repair signature that defines at least one cache array location associated with the processor design which has failed the cache test in a statistically relevant percentage of the processors in the lot *(column 5 lines 3-6 and column 6 lines 18-61)*.

Claim Rejections - 35 USC § 103

The following is a quotation of 35 U.S.C. 103(a) which forms the basis for all obviousness rejections set forth in this Office action:

> (a) A patent may not be obtained though the invention is not identically disclosed or described as set forth in section 102 of this title, if the differences between the subject matter sought to be patented and the prior art are such that the subject matter as a whole would have been obvious at the time the invention was made to a person having ordinary skill in the art to which said subject matter pertains. Patentability shall not be negatived by the manner in which the invention was made.

6. Claims 4, 10, and 12 are rejected under 35 U.S.C. 103(a) as being unpatentable over Song et al. in view of Edmondson et al. (U.S. Patent No. 5,680,544).

As in claims 4, 10, and 12 Song et al. teaches the limitations of claims 1, 7, and 11, respectively. However, Song et al. fails to teach of determining a column and row in a cache array. Edmondson et al. teaches determining the at least one cache array location comprises determining a column and row location in the corresponding cache array *(column 1 lines 61-63)*.

It would have been obvious to a person skilled in the art at the time the invention was made to have included the row and column determination as taught by Edmondson in the invention of Song et al. This would have been obvious because analyzing a cache memory in a

processor on a wafer at the memory bit level rather than at the cache array level allows for a more precise determination of the occurrence of a fault.

Conclusion

7. The prior art made of record and not relied upon is considered pertinent to applicant's disclosure:

U.S. PGPub 2005/0039089 Gedamu et al. discloses cache testing on a wafer.

8. Any inquiry concerning this communication or earlier communications from the examiner should be directed to Paul Contino whose telephone number is (571) 272-3657. The examiner can normally be reached on Monday-Friday 9:00 am - 6:00 pm.

If attempts to reach the examiner by telephone are unsuccessful, the examiner's supervisor, Scott Baderman can be reached on (571) 272-3644. The fax phone number for the organization where this application or proceeding is assigned is 571-273-8300.

Information regarding the status of an application may be obtained from the Patent Application Information Retrieval (PAIR) system. Status information for published applications may be obtained from either Private PAIR or Public PAIR. Status information for unpublished applications is available through Private PAIR only. For more information about the PAIR system, see http://pair-direct.uspto.gov. Should you have questions on access to the Private PAIR system, contact the Electronic Business Center (EBC) at 866-217-9197 (toll-free). If you would

like assistance from a USPTO Customer Service Representative or access to the automated information system, call 800-786-9199 (IN USA OR CANADA) or 571-272-1000.

PFC
8/2/2006

SCOTT BADERMAN
SUPERVISORY PATENT EXAMINER